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AN10273

Power MOSFET single-shot and repetitive avalanche ruggedness rating

Rev. 3 — 10 December 2015 **Application note**

Document information

Info	Content
Keywords	power MOSFET, single-shot, avalanche, ruggedness, safe operating condition
Abstract	Power MOSFETs are normally measured based on single-shot Unclamped Inductive Switching (UIS) avalanche energy. This application note describes in detail, the avalanche ruggedness performance, fundamentals of UIS operation and appropriate quantification method for the safe operating condition.

Revision history

Rev	Date	Description
3	20151210	Section 2: added

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1. Introduction

Electronic applications have progressed significantly in recent years and have inevitably increased the demand for an intrinsically rugged power MOSFET. Device ruggedness defines the capacity of a device to sustain an avalanche current during an unclamped inductive load switching event. The avalanche ruggedness performance of a power MOSFET is normally measured as a single-shot Unclamped Inductive Switching (UIS) avalanche energy or $E_{DS(AL)S}$. It provides an easy and quick method of quantifying the robustness of a MOSFET in avalanche mode. However, it does not necessarily reflect the true device avalanche capability (see Ref. 1, Ref. 2 and Ref. 3) in an application.

This application note explains the fundamentals of UIS operation. It reviews the appropriate method of quantifying the safe operating condition for a power MOSFET, subjected to UIS operating condition. The application note also covers the discussions on repetitive avalanche ruggedness capability and how this operation can be quantified to operate safely.

2. Single-shot and repetitive avalanche definitions

Single-shot avalanche events are avalanche events that occur due to a fault condition in the application such as electrical overstress. The application does not have an avalanche designed into its operation.

However, repetitive avalanche refers to the applications where avalanche is an intended operation mode of the MOSFET. Here, avalanche is a designed function and is independent of the number of avalanche events.

Any customer wishing to operate outside the current avalanche ratings may be considered on an application basis. Contact your local sales team for more information.

3. Understanding power MOSFET single-shot avalanche events

The researchers and the industry have established single-shot avalanche capability of a device (see Ref. 1, Ref. 2 and Ref. 3). The test is carried out on a simple unclamped inductive load switching circuit, as shown in Figure 1.

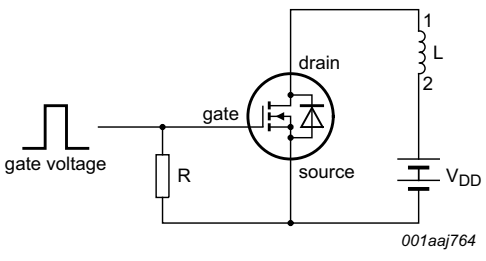

Fig 1. Unclamped inductive load test circuit for MOSFET ruggedness evaluation

3.1 Single-shot UIS operation

A voltage pulse is applied to the gate to turn on the MOSFET, as shown in Figure 2. It allows the load current to ramp up according to the inductor value (L) and the drain supply voltage (V_{DD}). The phenomenon is shown in Figure 3 and Figure 4. At the end of the gate

pulse, the MOSFET is turned off. The current in the inductor continues to flow, causing the voltage across the MOSFET to rise sharply. This overvoltage is clamped at breakdown voltage (V_{BR}) until the load current reaches zero, as illustrated in Figure 3. Typically, V_{BR} is:

$$V_{BR} \approx 1.3 \times V_{(BR)DSS} \tag{1}$$

The peak load current passing through the MOSFET before turn off is the non-repetitive drain-source avalanche current ($I_{DS(AL)S}$) of the UIS event. $I_{DS(AL)S}$ is illustrated in Figure 4. The following expression is used to determine the rate at which the avalanche current decays, which is dependent on the inductor value:

$$\frac{dI_{DS(AL)S}}{dt_{AL}} = -\frac{V_{BR} - V_{DD}}{L} \tag{2}$$

The peak drain-source avalanche power ($P_{DS(AL)M}$) dissipated in the MOSFET is shown in Figure 5. It is a product of the breakdown voltage (V_{BR}) and the non-repetitive drain-source avalanche current ($I_{DS(AL)S}$); see Figure 3 and Figure 4. The avalanche energy dissipated is the area under the P_{AV} waveform and is estimated from the following expression:

$$E_{DS(AL)S} = \frac{P_{DS(AL)M} \times t_{AL}}{2} \tag{3}$$

or

$$E_{DS(AL)S} = \frac{1}{2} \cdot \frac{V_{BR}}{V_{BR} - V_{DD}} \cdot LI^2_{DS(AL)S} \tag{4}$$

Another crucial parameter involved in a MOSFET avalanche event is the junction temperature. After the avalanche event (τ) has begun, the following expression is used to determine the transient junction temperature variation during device avalanche at a given time:

$$\Delta T_j(\tau) = \int_0^{\tau} P_{AV}(t) \frac{dZ_{th(\tau - t)}}{dt} dt \tag{5}$$

where Z_{th} is the power MOSFET transient thermal impedance. Alternatively, the following expression approximates the maximum ΔT_j:

$$\Delta T_{j(max)} \approx \frac{2}{3} P_{DS(AL)M} Z_{th(t_{AL}/2)} \tag{6}$$

Assuming that $T_{j(max)}$ occurs at $t_{AL}/2$, $Z_{th(t_{AL}/2)}$ is the transient thermal impedance measured at half the avalanche period t_{AL}.

Therefore, the maximum junction temperature resulting from the avalanche event is:

$$T_{j(max)} \approx \Delta T_{j(max)} + T_j \tag{7}$$

where T_j refers to the junction temperature prior to turn off.

3.1.1 Single-shot UIS waveforms

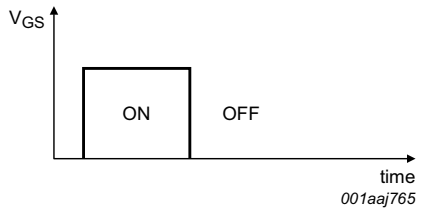

Fig 2. Gate-source voltage, V_{GS}

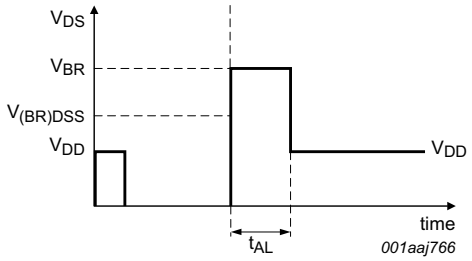

Fig 3. Drain-source voltage, V_{DS}

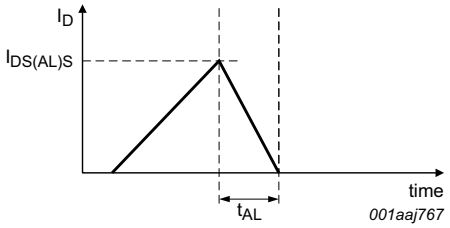

Fig 4. Drain current, I_D

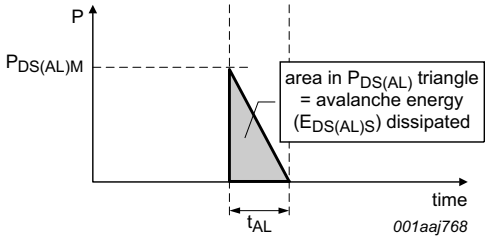

Fig 5. Peak drain-source avalanche power, $P_{DS(AL)M}$

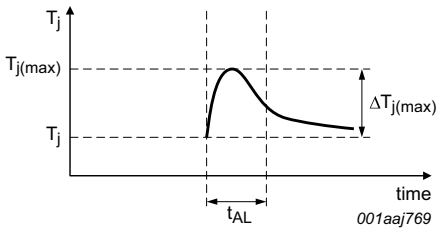

Fig 6. Transient junction temperature profile of MOSFET during an avalanche event

3.2 Single-shot avalanche ruggedness rating

The failure mechanism for a single-shot avalanche event in a power MOSFET is due to the junction temperature exceeding the maximum temperature rating. In such a case, catastrophic damage occurs to the MOSFET. If the transient temperature resulting from an avalanche event, as shown in Figure 6, rises beyond a recommended rated value, the device risks being degraded. The recommended rated value is derated from the maximum temperature for optimum reliability.

Blackburn (see Ref. 2) has discussed a general guideline in detail, on the appropriate method of quantifying the single-shot avalanche capability of a device. It takes the avalanche current and initial junction temperature into consideration. The maximum allowed avalanche current as a function of avalanche time defines the safe operation for a device single-shot UIS event. The maximum allowed avalanche current is set so that a safe maximum junction temperature, $T_{j(max)}$ of 175 °C, is never exceeded. Using Equation 7, Figure 7 is plotted.

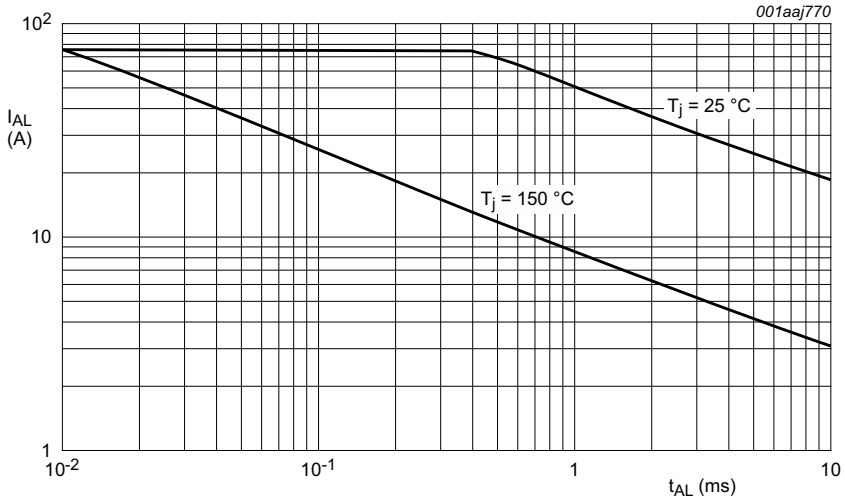

Fig 7. Single-shot avalanche ruggedness Safe Operating ARea (SOAR) curves of BUK764R0-55B limited to a $T_{j(max)}$ of 175 °C

Figure 7 shows the SOAR curves of a device single-shot avalanche capability. The 25 °C junction temperature curve shows the maximum allowable $I_{DS(AL)S}$ for a given t_{AL} at an initial T_j of 25 °C. This maximum I_{AL} results to a maximum allowable junction temperature $T_{j(max)}$ of 175 °C, which means a $\Delta T_{j(max)}$ of 150 °C.

The area under the SOAR curve is the Safe Operating ARea (SOAR). Similarly, the 150 °C junction temperature curve is the maximum operating limit for an initial T_j of 150 °C. The maximum value of $I_{DS(AL)S}$ induces a $\Delta T_{j(max)}$ of 25 °C, resulting in a $T_{j(max)}$ of 175 °C. Again the area under the curve is the SOAR.

The maximum junction temperature resulting in catastrophic device avalanche failure is approximately 380 °C, which is in excess of the rated $T_{j(max)}$ of 175 °C. However, operating beyond the rated $T_{j(max)}$ may induce long-term detrimental effects to the power MOSFET and is not recommended.

4. Understanding power MOSFET repetitive avalanche events

Repetitive avalanche refers to an operation involving repeated single-shot avalanche events, as discussed earlier. Until recently, most manufacturers have avoided the issues pertaining to the power MOSFET repetitive avalanche capability. It is primarily due to the complexity in such operations and the difficulties in identifying the underlying physical degradation process in the device.

Due to the traumatic nature of the avalanche event, a repetitive avalanche operation can be hazardous for a MOSFET. It is hazardous even when the individual avalanche events are below the single-shot UIS rating. This type of operation involves additional parameters such as frequency, duty cycle, and thermal resistances ($R_{th(j-a)}$ and $R_{th(j-mb)}$) of the system during the avalanche event. However, it is possible to derate the single-shot rating to define a repetitive avalanche SOAR.

4.1 Repetitive UIS operation

The repetitive UIS test circuit is shown in Figure 1. The gate is fed with a train of voltage pulses at a frequency (f) and for a duty cycle as shown in Figure 8. The resulting breakdown voltage (V_{BR}) and drain current (I_D) passing through the load are the same as for a single-shot UIS. However, the peak I_D is now denoted as repetitive drain-source avalanche current ($I_{DS(AL)R}$), as shown in Figure 9.

The repetitive drain-source avalanche power ($P_{DS(AL)R}$) resulting from the repetitive UIS operation is shown in Figure 10. For finding the value of $P_{DS(AL)R}$, it is necessary to first calculate $E_{DS(AL)S}$ for a single avalanche event using Equation 3. This resultant value of $E_{DS(AL)S}$ is substituted in the following expression, to calculate the value of $P_{DS(AL)R}$:

$$P_{DS(AL)R} = E_{DS(AL)S} \times f \tag{8}$$

4.1.1 Repetitive UIS waveforms

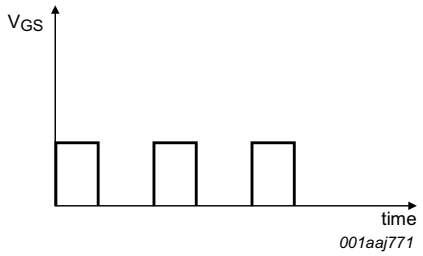

Fig 8. Gate pulse, V_{GS}

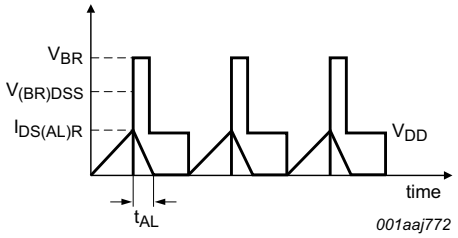

Fig 9. Drain-source voltage, V_{DS} and repetitive drain-source avalanche current, $I_{DS(AL)R}$

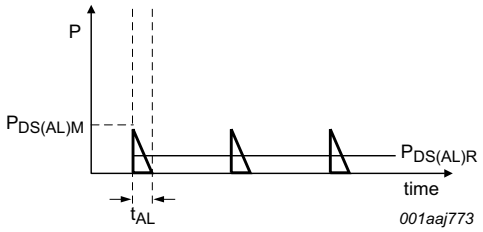

Fig 10. Repetitive drain-source avalanche power, $P_{DS(AL)R}$

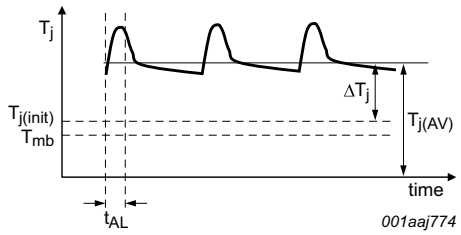

Fig 11. Transient junction temperature components of MOSFET during repetitive avalanche

4.2 Temperature components

The temperature rise from the repetitive avalanche mode in the power MOSFET is shown in Figure 11.

The temperature ($T_{j(init)}$) comprises the mounting base temperature (T_{mb}) and the temperature rise resulting from any on-state temperature difference (ΔT_{on}).

$$T_{j(init)} = T_{mb} + \Delta T_{on} \tag{9}$$

In addition, there is a steady-state average junction temperature variation (ΔT_j) resulting from the average repetitive avalanche power loss.

$$\Delta T_j = P_{DS(AL)R} \times R_{th(j\text{-}a)} \quad (10)$$

where $R_{th(j-a)}$ is the thermal resistance from junction to ambient of the device in the application. The summation of Equation 9 and Equation 10 gives the average junction temperature, $T_{j(AV)}$ of a power MOSFET in repetitive UIS operation.

$$T_{j(AV)} = T_{j(init)} + \Delta T_j \quad (11)$$

5. Repetitive avalanche ruggedness rating

Following extensive investigation, it is clear that there is more than one failure or wear-out mechanism involved in repetitive avalanche. Temperature is **not** the only limiting factor to a repetitive avalanche operation. However, by limiting temperature and the repetitive drain-source avalanche current ($I_{DS(AL)R}$), an operating environment is defined such that the avalanche conditions do not activate device degradation. It allows the power MOSFET to operate under repetitive UIS conditions safely.

Figure 12 shows the single-shot and repetitive avalanche SOAR curves of BUK764R0-55B, where 'Rep. Ava' represents the 'repetitive avalanche SOAR curve'.

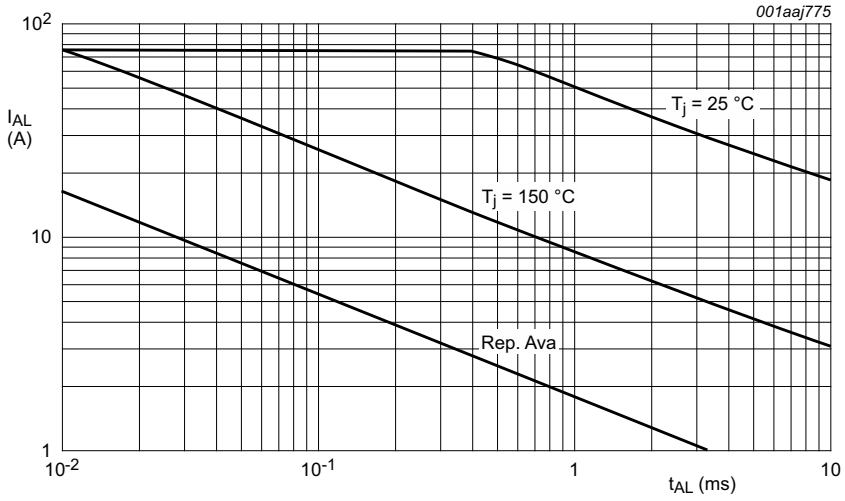

Fig 12. Single-shot and repetitive avalanche SOAR curves of BUK764R0-55B limited to $T_{j(max)}$ of 175 °C and $T_{j(AV)}$ of 170 °C, respectively

The two conditions which must be satisfied for safe operation of a power MOSFET under repetitive avalanche mode are:

1. $I_{DS(AL)R}$ should **not** exceed the repetitive avalanche SOAR curve
2. $T_{j(AV)}$ should **not** exceed 170 °C

6. Conclusion

Power MOSFETs can sustain single-shot and repetitive avalanche events. Simple design rules and SOAR regions are provided.

7. Examples

The following examples examine cases of avalanche operation acceptance:

7.1 Single-shot avalanche case

- Device: BUK764R0-55B; see Figure 12
- L = 2 mH
- $I_{DS(AL)S}$ = 40 A
- $R_{th(j-a)}$ = 5 K/W
- $V_{(BR)DSS}$ = 55 V
- V_{DD} = 0 V

7.1.1 Calculation steps

1. Using the above information, t_{AL} can be determined using Equation 2, which in this case is 1.11 ms. Transferring the I_{AL} and t_{AL} conditions onto Figure 12, the operating point is in between the T_j = 25 °C and T_j = 150 °C SOAR curves. It suggests that the operating condition may be feasible.
2. To check, calculate the $\Delta T_{j(max)}$ using Equation 6, where $Z_{th(556\ \mu s)}$ in the data sheet is approximately 0.065 K/W. It gives a $\Delta T_{j(max)}$ of 124.8 °C.

Based on the above calculations, the operating condition is acceptable if the device T_j < 50 °C.

7.2 Repetitive avalanche case

- Device: BUK764R0-55B; see Figure 12
- L = 0.5 mH
- $I_{DS(AL)R}$ = 6 A
- f = 3 kHz
- $R_{th(j-a)}$ = 5 K/W
- T_o = 100 °C
- $V_{(BR)DSS}$ = 55 V
- V_{DD} = 0 V

7.2.1 Calculation steps

1. From the above information, t_{AL} can be determined using Equation 2, which in this case is approximately 0.042 ms. Transferring the I_{AL} and t_{AL} conditions onto Figure 12, the operating point is under the boundary of the ‘Rep. Ava’ SOAR curve. It suggests that the operating condition is acceptable. Therefore, condition 1 is satisfied.
2. Calculate the non-repetitive drain-source avalanche energy ($E_{DS(AL)S}$) using Equation 3 ($E_{DS(AL)S}$ = 9 mJ).
3. Calculate the repetitive drain-source avalanche power ($P_{DS(AL)R}$) using Equation 8 ($P_{DS(AL)R}$ = 27 W).

4. Calculate the average ΔT_j rise from repetitive avalanche (ΔT_j) using Equation 10 (ΔT_j = 135 °C).
5. Determine the average junction maximum temperature in repetitive avalanche operation ($T_{j(AV)}$) using Equation 11 ($T_{j(AV)}$ = 235 °C). Therefore, condition 2 is not satisfied.

Based on the above calculations, the operating conditions meet the first requirement but not the second requirement for safe repetitive avalanche operation. It is because the maximum $T_{j(AV)}$ exceeded 170 °C.

To make the above operation viable, the design engineer has to satisfy the second condition by reducing $T_{j(AV)}$. It can be achieved by improving the heat sinking of the device. Reducing $R_{th(j-a)}$ from 5 K/W to 2.5 K/W gives a $T_{j(AV)}$ of 167.5 °C, satisfying condition 2 for safe repetitive avalanche operation.

8. Appendix A

The following table describes the symbols used throughout this application note.

Table 1. Description of symbols

Symbol	Description
$V_{(BR)DSS}$	drain-source breakdown voltage
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy
I_D	drain current
$I_{DS(AL)S}$	non-repetitive drain-source avalanche current
$I_{DS(AL)R}$	repetitive drain-source avalanche current
I_{AL}	avalanche current
L	inductance
$P_{DS(AL)M}$	peak drain-source avalanche power
$P_{DS(AL)R}$	repetitive drain-source avalanche power
$R_{th(j-a)}$	thermal resistance from junction to ambient
$R_{th(j-mb)}$	thermal resistance from junction to mounting base
$T_{j(init)}$	initial junction temperature[1]
ΔT_{on}	on-state temperature difference
T_j	junction temperature
ΔT_j	junction temperature variation
$\Delta T_{j(max)}$	maximum junction temperature variation
$T_{j(max)}$	maximum junction temperature
$T_{j(AV)}$	average junction temperature[2]
T_{mb}	mounting base temperature
t_{AL}	avalanche time
V_{BR}	breakdown voltage
V_{DS}	drain-source voltage
V_{GS}	gate-source voltage

Table 1. Description of symbols *...continued*

Symbol	Description
Z_{th}	transient thermal impedance
$Z_{th(t_{AL}/2)}$	transient thermal impedance[3]
V_{DD}	supply voltage

[1] Summation of T_{mb} and ΔT_{on}.

[2] For repetitive avalanche.

[3] Measured at half the avalanche period.

9. Abbreviations

Table 2. Abbreviations

Acronym	Description
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
SOAR	Safe Operating ARea
UIS	Unclamped Inductive Switching

10. References

[1] **Turn-Off Failure of Power MOSFETs —** D.L. Blackburn, Proc. 1985 IEEE Power Electronics Specialists Conference, pages 429 to 435, June 1985.

[2] **Power MOSFET failure revisited —** D.L. Blackburn, Proc. 1988 IEEE Power Electronics Specialists Conference, pages 681 to 688, April 1988.

[3] **Boundary of power-MOSFET, unclamped inductive-switching (UIS), avalanche-current capability —** Rodney R. Stoltenburg, Proc. 1989 Applied Power Electronics Conference, pages 359 to 364, March 1989.

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12. Tables

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